



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/473,394	12/28/1999	KAIZAD R. MISTRY	042390.P6892	9930

7590 09/24/2002

RAYMOND J WERNER
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES, CA 90025

[REDACTED] EXAMINER

KANG, DONGHEE

[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2811

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/473,394	MISTRY, KAIZAD R.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 01 July 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 10-22 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-9 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Acknowledgment

1. Applicant's Amendment and Response to Paper No.13 has been entered and made of Record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (US 6,303,448).

Regarding claim 1, Chang et al. teach a field effect transistor, comprising (Fig.6): a substrate (10) having a recess in a substrate thereof, the recess having a bottom portion and substantially vertical sidewalls; a gate dielectric layer (62) disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls; a gate electrode (64) completely overlying the gate dielectric layer; and source/drain terminals (70) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprises an extension (LDD) which extends to a more shallow depth within the substrate than the source/drain terminals to which it

corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, a portion of the gate dielectric layer overlying an innermost portion of the extension.

Regarding claim 2, Chang et al. teach the transistor further comprising a portion of the gate electrode that overlies the innermost portion of the source/drain extension.

Regarding claim 3, Chang et al. teach the gate electrode conforms to the recessed channel.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 6,303,448) in view of Hwang (US 5,567,966).

Regarding claim 4, Chang et al. teach a field effect transistor, comprising (Fig.6): a substrate (10) having a recess in a substrate thereof, the recess having a bottom portion and substantially vertical sidewalls; a gate dielectric layer (62) disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls; a gate electrode (64) completely overlying the gate dielectric layer; and source/drain terminals (70) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed;

wherein the source/drain terminals comprises an extension (LD) which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, a portion of the gate dielectric layer overlying an innermost portion of the extension.

Chang et al. use etching method to form the recess, which has a bottom portion and vertical sidewalls. However, Chang et al. does not explicitly teach the recess having tapered sidewalls resulted from the use of oxidation method. However, Hwang teaches using oxidation method to form the recess having a bottom portion and tapered sidewalls, the tapered sidewall surface forming an obtuse angle with respect to the bottom portion of the recess (see Fig.1-6 & Col.1, lines 50-56). Therefore, it would have been obvious in the art at the time the invention was made to form the recess using oxidation method as taught by Hwang instead of etching method of Chang et al., since oxidation method is capable of producing SiO₂ with controlled thickness so as to obtain the desired thinned channel region.

Regarding claim 5, Chang et al. as modified by Hwang teach the transistor further comprising a portion of the gate electrode that overlies the innermost portion of the source/drain extension.

Regarding claim 6, Chang et al. as modified by Hwang teach the gate electrode conforms to the recessed channel.

6. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 5,712,503) in view of Chang et al. (US 6,303,448).

Regarding claim 7, Kim et al. teach a field effect transistor, comprising (Fig.4L):
a substrate (51) having a recess in a surface thereof, the recess having a curvilinear shape; a gate dielectric layer (62) disposed superjacent the curvilinear recess; a gate electrode completely overlying the gate dielectric layer; and source/drain terminals (65) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprises an extension (60) and a portion of the gate dielectric layer overlaying an inner-most portion of the extension.

Kim et al. does not teach the extension extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds.

Electric fields tend to be increased at small geometries, since device voltages are difficult to scale to arbitrarily small values. As a result, various hot carrier effects appear in short-channel devices. It is well known in the art that forming the lightly doped drain (LDD) structure which decreases the field between the drain and channel regions, thereby reducing injection into the oxide, impact ionization, and other hot electron effects. The LDD uses two doping levels, with heavy doping over most of the source and drain areas but with light doping in a region adjacent to the channel where the depth of heavily-doped region can be made somewhat greater than lightly-doped region without adversely impacting the device operation and gate electrode overlies an innermost portion of the source/drain extension since it is further away from the channel

and also taught by Chang et al. in Fig.6. The increased junction depth lowers both the sheet resistance and the contact resistance of the drain. Hence it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Chang et al. with Kim et al.'s device to have the shallow lightly-doped region since it absorbs some of the potential into the drain and thus decreases the electric field.

Regarding claim 8, Kim et al. as modified by Chang et al. teach the transistor further comprising a portion of the gate electrode that overlies the innermost portion of the source/drain extension.

Regarding claim 9, Kim et al. as modified by Chang et al. teach the gate electrode conforms to the recessed channel.

Response to Arguments

7. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

Art Unit: 2811

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DHK
September 18, 2002

Steve Lohr
Patent Examiner
Steve Lohr